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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/709,923	06/07/2004	Min-Lung Huang	10788-US-PA	3922

31561 7590 11/20/2008

JIANQ CHYUN INTELLECTUAL PROPERTY OFFICE
7 FLOOR-1, NO. 100
ROOSEVELT ROAD, SECTION 2
TAIPEI, 100
TAIWAN

EXAMINER	
CHAMBLISS, ALONZO	
ART UNIT	PAPER NUMBER
2892	

NOTIFICATION DATE	DELIVERY MODE
11/20/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

USA@JCIPGROUP.COM.TW
Belinda@JCIPGROUP.COM.TW

Office Action Summary	Application No.	Applicant(s)	
	10/709,923	HUANG ET AL.	
	Examiner	Art Unit	
	Alonzo Chambliss	2892	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 August 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *7-11 and 13-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *7-11 and 13-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 June 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. The amendment filed on 8/28/08 has been fully considered and made of record in the instant application.

2. The rejection mailed on 5/30/08 has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Dalal et al. (US 5,796,591) and JP 62-117346).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

4. Claims 7, 8, 10, and 14-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Horikoshi et al. (JP 62-117346) in view of Asai et al. (US 6,534,723).

With respect to Claim 15, Horikoshi discloses providing a substrate 21 having a first surface and an opposite second surface wherein the substrate 21 includes a plurality of first contacts 22 on the first surface of the substrate 21. Forming a plurality of bumps 24 on the first surface of the substrate 21, wherein each bump 24 is connected to one first contact 22, wherein the bumps 24 has a first melting point. A chip 26 having a plurality of bonding pads 27 corresponding to the bumps 24, wherein a metal layer 28 is disposed on surfaces of the bonding pads 27. A conductive adhesive layer 29 on the metal layer 28, wherein the conductive adhesive layer 29 has a second melting point lower than the first melting point of the bumps 24. Arranging the chip 26 onto the first surface of the substrate by flipping the chip, so that the bonding pads 27 with the adhesive layer are connected to the bumps 24. Reflowing the conductive adhesive layer 29 for wrapping the top portion of the bumps 24 wherein the bumps remain not melted (see English abstract and Figs. 1-4). Horikoshi fails to disclose a plurality of second contacts on the second surface of the substrate 10. The first contacts are electrically connected to the second contacts. However, Asai discloses a plurality of second contacts 40 or 94 on the second surface of the substrate 34, 46, 50, 52 and 54 or 60, 65,106, 108, and 90. The first contacts 40 or 94 are electrically connected to the second contacts 40 or 94 (see Figs. 7 and 18). Thus, Horikoshi and Asai have substantially the same environment of a chip mounted and electrically connected to a substrate by solder bumps. Therefore, one skilled in the art at the time of invention was made would readily recognize incorporating second contacts on the second surface of the substrate of Horikoshi, since the second contacts would allow the chips on the first surface to be electrically connected to the motherboard facing the second side of the substrate as taught by Asai.

With respect to Claims 7 and 8, Asai discloses disposing a plurality of solder balls or pins 64 or 66 on the second surface of the substrate, wherein the solder balls or pins are connected to the second contacts (see Figs.7, 8, and 10).

With respect to Claim 10, Asai discloses forming the bumps comprises printing a tin paste onto surfaces of the first contacts and reflowing the tin paste (see col. 18 lines 48-56, col. 19 lines 58-67, and col. 26 lines 45-50).

With respect to Claim 14, Asai discloses wherein the metal layer is a nickel layer formed by electroless plating (see col. 19 lines 55-67; Figs. 7-10).

With respect to Claim 16, Horikoshi discloses wherein each of the bumps has a smooth curving top surface (see Figs. 3 and 4).

5. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Horikoshi et al. (JP 62-117346) and Asai et al. (US 6,534,723) as applied to claim 15 above, and further in view of Acocella et al. (US 5,591,941).

With respect to Claim 9, Horikoshi-Asai discloses the claimed invention except for forming the bumps comprising implanting tin globes and treating surfaces of the first contacts with a flux before implanting tin globes. However, Acocella discloses forming the bumps 18 comprising implanting tin globes and treating surfaces of the first contacts with a flux before implanting tin globes (see col. 5 lines 20-59; Fig. 5). Thus, Asai-Horikoshi-Asai and Acocella have substantially the same environment of bumps formed on a substrate. Therefore, one skilled in the art at the time of the invention would readily recognize incorporating a flux on the first contact pad of Horikoshi-Asai, since

the flux would facilitate connection between the bump and the contact pad as taught by Acocella.

6. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Horikoshi et al. (JP 62-117346) and Asai et al. (US 6,534,723) as applied to claim 15 above, and further in view of Sakuyama et al. (US 5,591,941).

With respect to Claim 13, Hirokoshi-Asai discloses the claimed invention except for filling an underfill material between the chip and the substrate, wherein the underfill material covers the bumps. However, Sakuyama discloses filling an underfill material 72 between the chip and the substrate, wherein the underfill material covers the bumps (see Fig. 5). Thus, Hirokoshi-Asai and Sakuyama have substantially the same environment of chip mounted and electrically connected to a substrate by bumps. Therefore, one skilled in the art at the time of invention would readily recognize incorporating an underfill material material between the chip and substrate of Hirokoshi-Asai, since the underfill material would improve the solder ball connection and coefficient of thermal expansion between the chip and substrate.

7. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Horikoshi et al. (JP 62-117346) and Asai et al. (US 6,534,723 as applied to claim 15 above, and further in view of Gansauge et al. (US 5,244,833).

With respect to Claim 11, Horikoshi-Asai discloses the claimed invention except for forming the bumps on surface of the first contacts by electroplating, thus forming the bumps on the substrate without reflowing. However, Gansauge discloses forming the bumps on surface of the first contacts by electroplating, thus forming the bumps on the

substrate without reflowing (see col. 4 lines 7-13 and col. 5 lines 40-45). Thus, Horikoshi-Asai and Gansauge have substantially the same environment of bumps formed on a substrate. Therefore, one skilled in the art at the time of the invention would readily recognize substitute an electroplating process for process used by Horikoshi-Asai to form the bumps, since the electroplating process would facilitate connection between the bump and the contact pad as taught by Gansauge.

The prior art made of record and not relied upon is cited primarily to show the process of the instant invention.

Conclusion

8. Any inquiry concerning the communication or earlier communications from the examiner should be directed to Alonzo Chambliss whose telephone number is (571) 272-1927.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thao Le can be reached on (571) 272-1708. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system Status information for published applications may be obtained from either Private PMR or Public PMR. Status information for unpublished applications is available through Private PMR only. For more information about the PMR system see http://pair-dkect.uspto.gov. Should you

have questions on access to the Private PMR system contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free) or EBC_Support@uspto.gov.

AC/November 14, 2008

/Alonzo Chambliss/
Primary Examiner, Art Unit 2892